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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,169	07/14/2003	Francisco Javier Guerrero Mercado	P05514 (NAT115-05514)	5012

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,169	GUERRERO MERCADO, FRANCISCO JAVIER	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12 and 14-19* is/are rejected.

7)☒ Claim(s) *5,13 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/10/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of "the pulsed bias curent comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock" of claims 7 and 15, "a current source biased by the pulsed or continuous bias current and controlled by the input signal" of claim 19 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 7-8 and 15-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In this instant, the specification has failed to describe as to how "the pulsed bias curent comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock" of claim 7 is made and/or used. Page 13, lines 12-14 of the specification has briefly mentioned that "pulse generator produces a 390ns wide pulse on every falling edged of the clk signal, and the comparator output out is sampled with the clk signal's rising edge". Figure 3 shows a black box labeled as "Pulse Generator" 301. A careful examination of the box 301, it is noted that there is not clock signal being shown. Similarly, the comparator 100 does not show the clock signal. Therefore, it is unclear as to how the pulsed bias curent comprises a pulse at one edge of **a system clock** and an output of the comparator is sampled at **another edge of the system clock** is performed. Clarification and correction are required.

Regarding claims 8 and 17, the specification fails to describe as to how "the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased a bias current with a different second level value" is enabled. Page 11, lines 6-25; page 12, lines 1-25

of the specification uses waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. However, it is unclear as to how the circuit shown in figures 4A and 4B enable operatively in first and second modes as called for in claim 8. That is, it is unclear as to how the comparator is selected to operate in a first mode in which the input gain stage is biased by a bias current with a defined first level value or when the comparator is selected to operate in a second mode the input gain stage is biased a bias current with a different second level value. Applicant is required to particularly point out the recited features.

Claims 15 and 16 are rejected for the same reasons as claims 7 and 8, respectively.

Regarding claim 19, the specification fails to describe as to how the "current source biased by the pulsed or continuous bias current and controlled the input signal" is enabled. Figure 1 shows **"an equivalent circuit"** of the actual present invention. The equivalent circuit shows a symbol of a variable current (ibias) being received a symbolic gm signal. Page 11, lines 6-25; page 12, lines 1-25 of the specification uses waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. However, it is unclear as to how the current source being biased by the pulse or continuous bias current and controlled by the input current would correspond to the actual components of the actual comparator shown in figures 4A and 4B. Therefore, it is unclear as to how current source biased by the pulsed or continuous bias current and controlled the input signal" is enabled.

Claims 18 and 20 are rejected under 35USC 112, first paragraph because of the technical deficiencies of claim 17.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeuchi (USP 5,708,673). Figure 5 of Ikeuchi shows an integrated circuit comparator comprising an input receiving an input signal (bases of transistors Q5, Q6) representative of a difference between quantities to be compared (Dt and Vref), an input gain stage (42) receiving the input signal and biased with a pulsed bias current (6), the input gain stage producing a gain based upon the input signal as called for in claims 1 and 9.

Regarding claims 2 and 10 the input signal is a current representative of transconductance of a differential pair of input transistors (Q1, Q2).

Regarding claims 3 and 11, the input gain stage further comprises a current source (Q7) biased by the pulsed bias current (6) and controlled by the input signal.

6. Claims 1-4, 6, 9-12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by To et al. (USP 6,051,999). Figure 7 of To et al. shows an integrated circuit comparator comprising an input receiving an input signal (current along drain/source of transistors 716 and 718) representative of a difference between quantities to be compared (Vin-, Vin+), an input gain stage (724, 726) receiving the input signal and biased with a pulsed bias current (620), the input gain stage producing a gain based upon the input signal as called for in claims 1, 9.

Regarding claims 2 and 10, the input signal is a current representative of

transconductance of a differential pair of input transistors (716 and 718).

Regarding claims 3 and 11, the input gain stage further comprises a current source (728) biased by the pulsed bias current (720) and controlled by the input signal.

Regarding claims 4 and 12 a voltage limiter (720, 722 are transistor connected diode) limiting to a voltage drop equals a threshold voltage of the transistors, a hysteresis circuit (feed back crossed coupled transistors 734, 736 provide hysteresis characteristic) coupled to an output of the input gain stage to reduce spurious output transitions when the pulsed bias current changes state.

Regarding claims 6 and 14, an output gain stage (latch 622 shown in figure 6) uses low threshold voltage transistors (column 9, lines 9-15), therefore, its propagation delay is negligible with respect to a propagation delay of the input stage having high threshold voltage transistors.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 8-9 and 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Hughes (US 2004/0164802A1). Figure 1 shows an integrated circuit comparator comprising an input receiving an input signal (current along collector/emitter of transistors 11 and 13) representative of a difference between quantities to be compared (33, 34), an input gain stage (21, 41, 42, 16) receiving the input signal and biased with a pulsed bias current (signals 36 and 37), the input gain stage producing a gain based upon the input signal as called for in claims 1, 9 and 17-19.

Regarding claims 8 and 16, the comparator selectively operates in a first mode (transistors 21 and 24 are off) in which the gain stage is biased by a bias current (16) with a defined first level value or in a second mode in which the input gain stage is biased a bias current with a different second level value (when the transistors 21 and 22 are on).

Allowable Subject Matter

8. Claims 5, 13 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

9/5/2004